REMARKS

Reconsideration of the present application is respectfully requested. Claims 1-14 are pending herein, with claims 9-14 previously withdrawn from consideration in response to a restriction requirement. Thus claims 1-8 and 15 are under consideration at the present time, as new claim 15 added herein.

Claims 1-5, 7 and 8 stand rejected under 35 U.S.C. §102(b) as anticipated by Kepler et al., U.S. Patent No. 6,100,145. According to the examiner, Kepler et al. teaches a method of fabricating a semiconductor device, comprising, *inter alia*, a second step (b) in which a first thermal annealing is *inherently provided* to the substrate. According to the examiner, this step is inherently practiced to the source/drain regions of the device.

The applicants respectfully disagree with the examiner's "inherency" contention concerning the first thermal annealing. First of all, the examiner implicitly recognizes that Kepler et al. does not teach annealing subsequent to applying a non-conductive oxide film, and thus he must contend the annealing step is inherent. However, the present specification shows that formation of the source/drain regions 108 take place prior to depositing the oxide film, as disclosed in the present specification at page 2, line 9, page 4, lines 4-6, and page 9, lines 6-9. Furthermore, Kepler et al. itself is consistent on this point, as Kepler et al. specifically states at col. 4, lines1-4 that

> According to the methodology of the present invention, a buffer layer of silicon is blanket deposited on a substrate after forming the source/drain implants, i.e., on source/drain regions and also on field oxide regions, gates and spacers.

Thus, if the examiner's rationale were correct, it appears that annealing would "implicitly" occur in Kepler et al's process earlier than as contended in the office action, as

the formation of source/drain regions takes place prior to fabrication of the substrate. Thus, it should be evident, with source drain regions formed earlier in both Kepler et al's disclosure and in the disclosure of the present process, that there is no basis whatsoever for the examiner to contend that it is inherent in Kepler et al. to practice a first thermal annealing, after oxide film formation over the semiconductor substrate, as set forth in claim 1. For this reason, it is the applicant's position that the first thermal annealing after oxide layer formation is not necessarily present in Kepler et al.

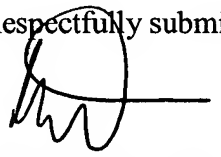
Furthermore, the reference does not teach an annealing step subsequent to depositing of the metal layer.

Accordingly, for these reasons, we are of the opinion that the §102(b) rejection based on Kepler et al. can be overcome with the arguments set forth herein.

Also, claim 6 is rejected under 35 U.S.C. §103(a) as unpatentable over Kepler et al. in view of Huang and Jeng. These references do not cure the deficiencies with respect to the Kepler reference.

Wherefore, based upon the foregoing, it is respectfully submitted that the present application is in condition of allowance and a relatively early reply is requested.

Respectfully submitted,



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